



Model Name: P650HVN02.0

Issue Date : 2011/09/20

(*)Preliminary Specifications

()Final Specifications

Customer Signature	Date	AUO	Date
Approved By _____		Approval By PM Director <i>Michael Goan</i> _____	
Note		Reviewed By RD Director <i>Eugene Chen</i> _____	
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Record of Revision

Version	Date	Page	Description
1.0	2011/07/27		First release
2.0	2011/08/18	6	Power Consumption: Typical TBD=>18.72, Max. TBD=>23.16 Inrush Current: Max TBD=>7.5 Backlight Power Consumption: Typical TBD=>209.6, Max. TBD=>229.9
		15	Add Note (3)
		16~18	These 3 paged are updated.
		23~24	Add drawings
		29	Pallet and Shipment Information is updated.
3.0	2011/9/20	6	IDD Min 0.6 => --, Typ.1.2 => 1.56, Max. 1.8 => 1.93
		6	F _{CLK} = 82MHz => 80.74MHz
		9	PIN 44, 46, 47
		10	PIN 40, 41
		10	Note 4 is deleted
		12	Vertical Section: Period Min 1090=>1096 Banking Min 10=>16
		16	Some items are deleted and notes are modified.
		17	PIN 13,14
		18	Includes 5% => less than 5%



1. General Description

This specification applies to the 64.5 inch Color TFT-LCD Module P650HVN02.0. This LCD module has a TFT active matrix type liquid crystal panel 1920 x 1080 pixels, and diagonal size of 64.5 inch. This module supports 1920 x 1080 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.

The P650HVN02.0 has been designed to apply the 10-bit 4 channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important.

* General Information

Items	Specification	Unit	Note
Active Screen Size	64.53	inch	
Display Area	1428.48 (H) x 803.52 (V)	mm	
Outline Dimension	1508.0(H) x 878.0(V) x 12.8(D)	mm	
Driver Element	a-Si TFT active matrix		
Display Colors	10 bit, 1.07B	Colors	
Number of Pixels	1920 x 1080	Pixel	
Pixel Pitch	0.744	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	Anti-Glare, 3H		Haze 2%

2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit

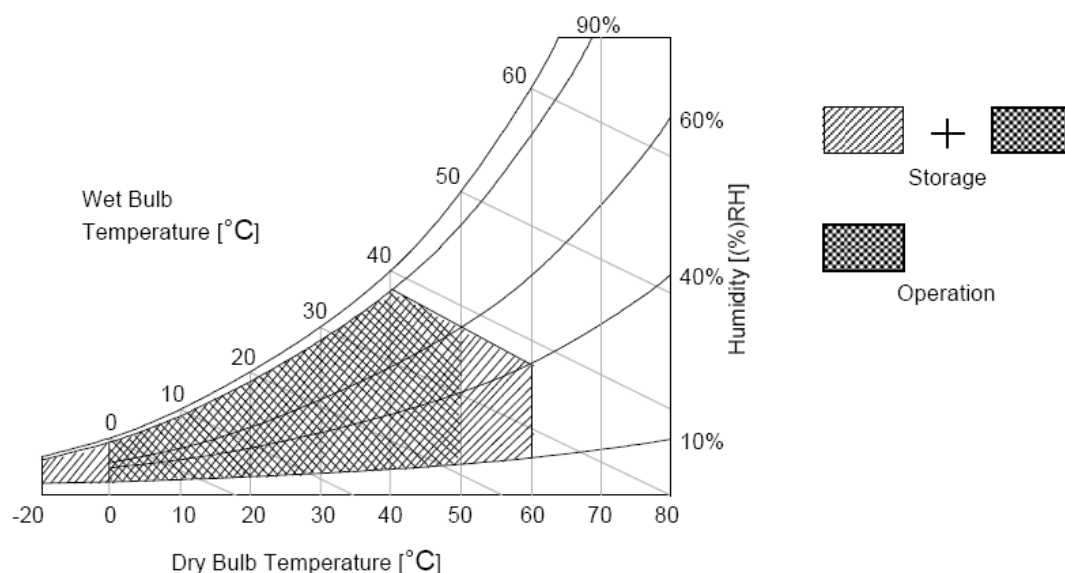
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	V_{in}	-0.3	4	[Volt]	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST	-	65	[°C]	Note 3

Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39°C and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40°C or less. At temperatures greater than 40°C, the wet bulb temperature must not exceed 39°C.

Note 3: Surface temperature is measured at 50°C Dry condition



3. Electrical Specification

The P650HVN02.0 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input for BLU is to **LED driver**.

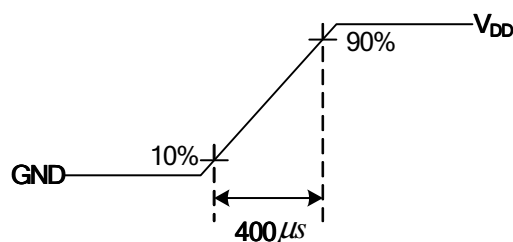
3.1 Electrical Characteristics

3.1.1: DC Characteristics

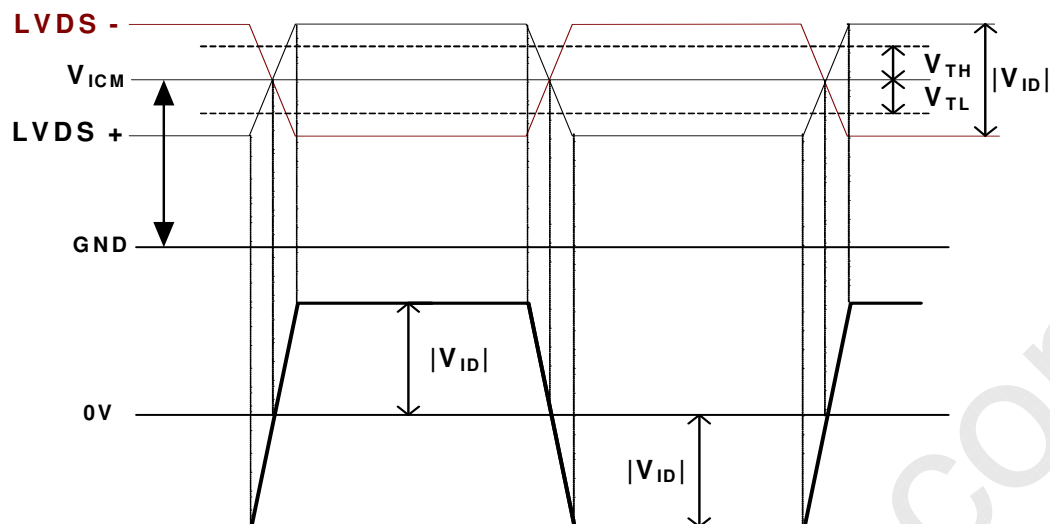
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LCD							
Power Supply Input Voltage		V_{DD}	10.8	12.0	13.2	V_{DC}	1
Power Supply Input Current		I_{DD}	--	1.56	1.93	A	2
Power Consumption		P_C	--	18.72	23.16	Watt	2
Inrush Current		I_{RUSH}	--	--	7.5	A	3
LVDS Interface	Input Differential Voltage	$ V_{ID} $	200	400	600	mV_{DC}	4
	Differential Input High Threshold Voltage	V_{TH}	+100	--	+300	4	4
	Differential Input Low Threshold Voltage	V_{TL}	-300	--	-100	4	4
	Input Common Mode Voltage	V_{ICM}	1.10	1.25	1.40	V_{DC}	4
CMOS Interface	Input High Threshold Voltage	V_{IH} (High)	2.7	--	3.3	V_{DC}	--
	Input Low Threshold Voltage	V_{IL} (Low)	0	--	0.6	V_{DC}	--
Backlight Power Consumption		P_{BL}	--	209.6	229.9	Watt	--
Life Time			30,000		--	Hours	--

Note :

1. The ripple voltage should be controlled under 10% of V_{CC}
2. $V_{DD} = 12.0V$, $F_v = 120Hz$, $F_{CLK} = 80.74MHz$, $25^\circ C$, Test Pattern : White Pattern
>> refer to "Section:3.3 Signal Timing Specification, Typical timing"
3. Measurement condition : Rising time = 400us



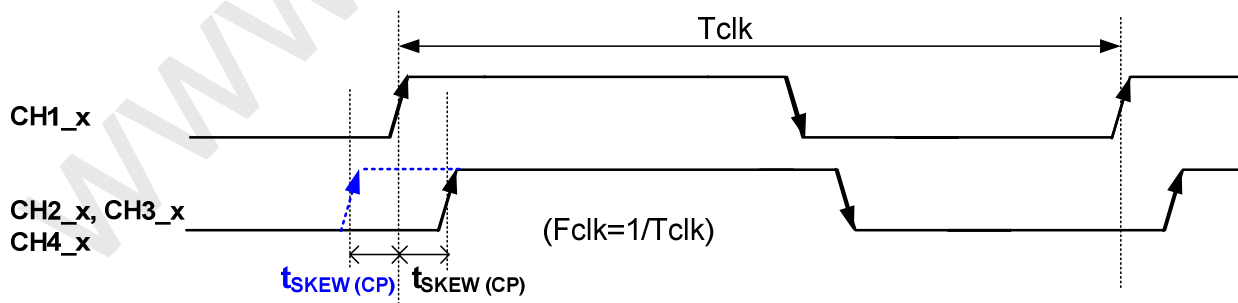
4. $V_{ICM} = 1.25V$



3.1.2: AC Electrical Characteristics

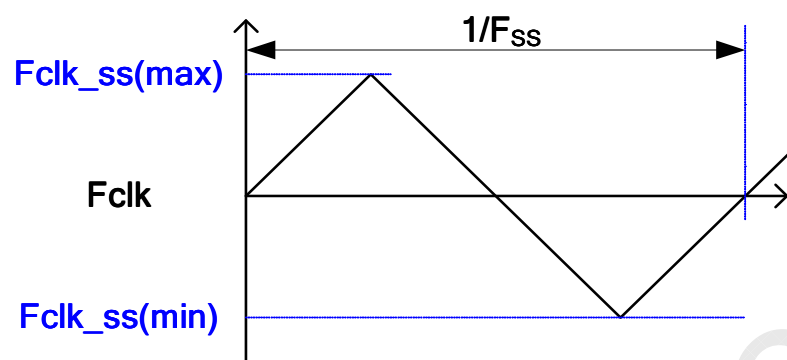
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Input Channel Pair Skew Margin	$t_{SKEW (CP)}$	-500	--	+500	ps	1
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	2
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	2
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	-0.4 -0.5	-- --	0.4 0.5	ns	3

1. Input Channel Pair Skew Margin



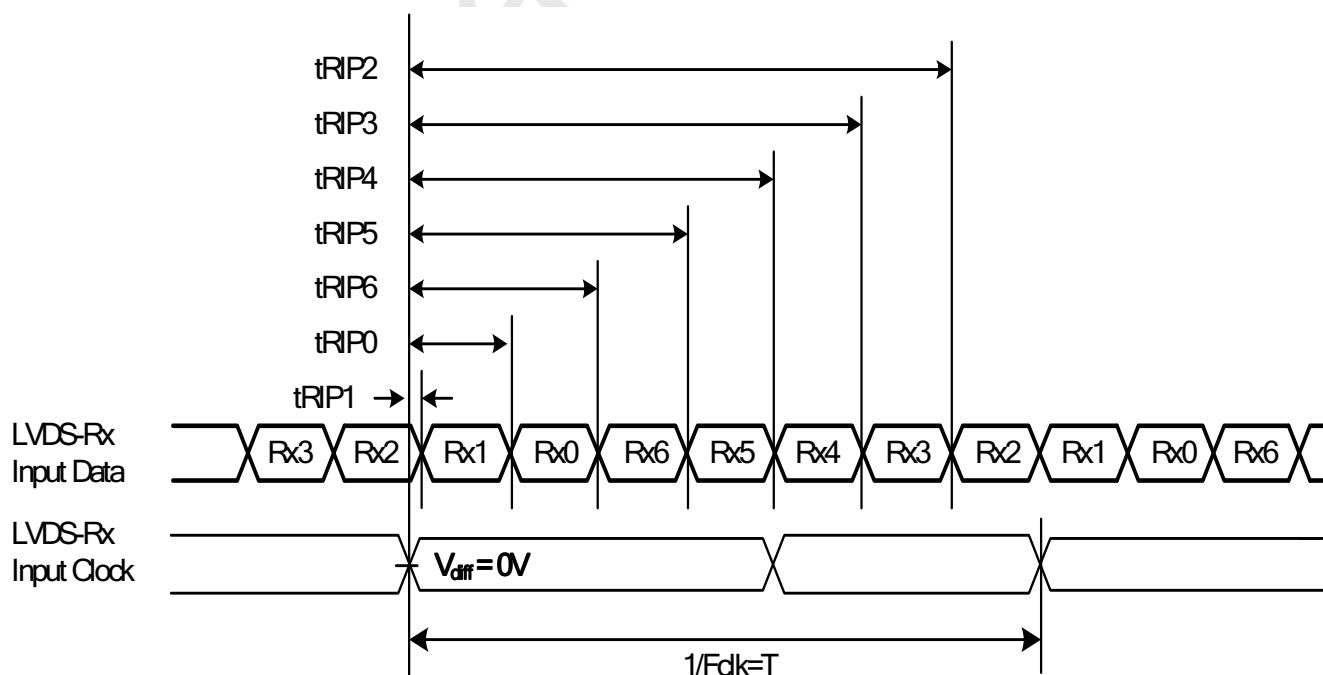
Note: x = 0, 1, 2, 3, 4

2. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures



3. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	$T=1/F_{clk}$
Input Data Position0	tRIP1	- tRMG	0	tRMG	ns	
Input Data Position1	tRIP0	$T/7 - tRMG $	$T/7$	$T/7 + tRMG $	ns	
Input Data Position2	tRIP6	$2T/7 - tRMG $	$2T/7$	$2T/7 + tRMG $	ns	
Input Data Position3	tRIP5	$3T/7 - tRMG $	$3T/7$	$3T/7 + tRMG $	ns	
Input Data Position4	tRIP4	$4T/7 - tRMG $	$4T/7$	$4T/7 + tRMG $	ns	
Input Data Position5	tRIP3	$5T/7 - tRMG $	$5T/7$	$5T/7 + tRMG $	ns	
Input Data Position6	tRIP2	$6T/7 - tRMG $	$6T/7$	$6T/7 + tRMG $	ns	



3.2 Interface Connections

LCD connector: FI-RE51S-HF (Manufactured by JAE)

Mating connector: FI-RE51S-HL (Manufactured by JAE)

PIN	Symbol	Description	PIN	Symbol	Description
1	VDD	Power Supply, +12V DC Regulated	26	CH4_0+	LVDS Channel 4, Signal 0+
2	VDD	Power Supply, +12V DC Regulated	27	CH4_1-	LVDS Channel 4, Signal 1-
3	VDD	Power Supply, +12V DC Regulated	28	CH4_1+	LVDS Channel 4, Signal 1+
4	VDD	Power Supply, +12V DC Regulated	29	CH4_2-	LVDS Channel 4, Signal 2-
5	VDD	Power Supply, +12V DC Regulated	30	CH4_2+	LVDS Channel 4, Signal 2+
6	GND	Ground	31	GND	Ground
7	GND	Ground	32	CH4_CLK-	LVDS Channel 4, Clock -
8	GND	Ground	33	CH4_CLK+	LVDS Channel 4, Clock +
9	GND	Ground	34	GND	Ground
10	CH2_0-	LVDS Channel 2, Signal 0-	35	CH4_3-	LVDS Channel 4, Signal 3-
11	CH2_0+	LVDS Channel 2, Signal 0+	36	CH4_3+	LVDS Channel 4, Signal 3+
12	CH2_1-	LVDS Channel 2, Signal 1-	37	CH4_4-	LVDS Channel 4, Signal 4-
13	CH2_1+	LVDS Channel 2, Signal 1+	38	CH4_4+	LVDS Channel 4, Signal 4+
14	CH2_2-	LVDS Channel 2, Signal 2-	39	GND	Ground
15	CH2_2+	LVDS Channel 2, Signal 2+	40	Reserve	AUO Internal Use Only
16	GND	Ground	41	Reserve	AUO Internal Use Only
17	CH2_CLK-	LVDS Channel 2, Clock -	42	Reserve	AUO Internal Use Only
18	CH2_CLK+	LVDS Channel 2, Clock +	43	Reserve	AUO Internal Use Only
19	GND	Ground	44	LD_EN	L or Open: Local Dimming Disable H (3.3V): Local Dimming Enable
20	CH2_3-	LVDS Channel 2, Signal 3-	45	LVDS_SEL	Open/High(3.3V) for NS, Low(GND) for JEIDA
21	CH2_3+	LVDS Channel 2, Signal 3+	46	Reserve	AUO Internal Use Only
22	CH2_4-	LVDS Channel 2, Signal 4-	47	Reserve	AUO Internal Use Only
23	CH2_4+	LVDS Channel 2, Signal 4+	48	BITSEL	Open/High(3.3V) for 10bit, Low(GND) for 8bit
24	GND	Ground	49	Reserve	AUO Internal Use Only
25	CH4_0-	LVDS Channel 4, Signal 0-	50	Reserve	AUO Internal Use Only
			51	Reserve	AUO Internal Use Only



LCD connector: FI-RE41S-HF (Manufactured by JAE)

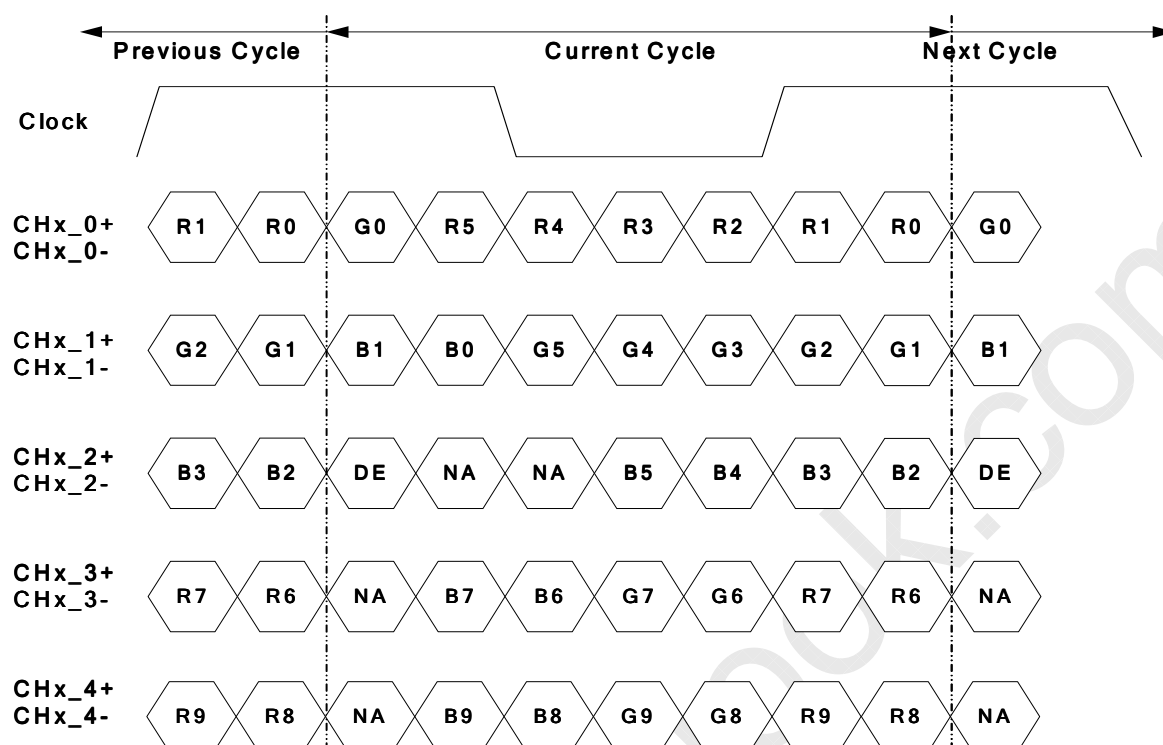
Mating connector: FI-RE41S-HL (Manufactured by JAE)

PIN	Symbol	Description	PIN	Symbol	Description
1	V _{DD}	Power Supply, +12V DC Regulated	21	CH1_3+	LVDS Channel 1, Signal 3+
2	V _{DD}	Power Supply, +12V DC Regulated	22	CH1_4-	LVDS Channel 1, Signal 4-
3	V _{DD}	Power Supply, +12V DC Regulated	23	CH1_4+	LVDS Channel 1, Signal 4+
4	V _{DD}	Power Supply, +12V DC Regulated	24	GND	Ground
5	V _{DD}	Power Supply, +12V DC Regulated	25	CH3_0-	LVDS Channel 3, Signal 0-
6	GND	Ground	26	CH3_0+	LVDS Channel 3, Signal 0+
7	GND	Ground	27	CH3_1-	LVDS Channel 3, Signal 1-
8	GND	Ground	28	CH3_1+	LVDS Channel 3, Signal 1+
9	GND	Ground	29	CH3_2-	LVDS Channel 3, Signal 2-
10	CH1_0-	LVDS Channel 1, Signal 0-	30	CH3_2+	LVDS Channel 3, Signal 2+
11	CH1_0+	LVDS Channel 1, Signal 0+	31	GND	Ground
12	CH1_1-	LVDS Channel 1, Signal 1-	32	CH3_CLK-	LVDS Channel 3, Clock -
13	CH1_1+	LVDS Channel 1, Signal 1+	33	CH3_CLK+	LVDS Channel 3, Clock +
14	CH1_2-	LVDS Channel 1, Signal 2-	34	GND	Ground
15	CH1_2+	LVDS Channel 1, Signal 2+	35	CH3_3-	LVDS Channel 3, Signal 3-
16	GND	Ground	36	CH3_3+	LVDS Channel 3, Signal 3+
17	CH1_CLK-	LVDS Channel 1, Clock -	37	CH3_4-	LVDS Channel 3, Signal 4-
18	CH1_CLK+	LVDS Channel 1, Clock +	38	CH3_4+	LVDS Channel 3, Signal 4+
19	GND	Ground	39	GND	Ground
20	CH1_3-	LVDS Channel 1, Signal 3-	40	Reserve	AUO Internal Use Only
			41	Reserve	AUO Internal Use Only

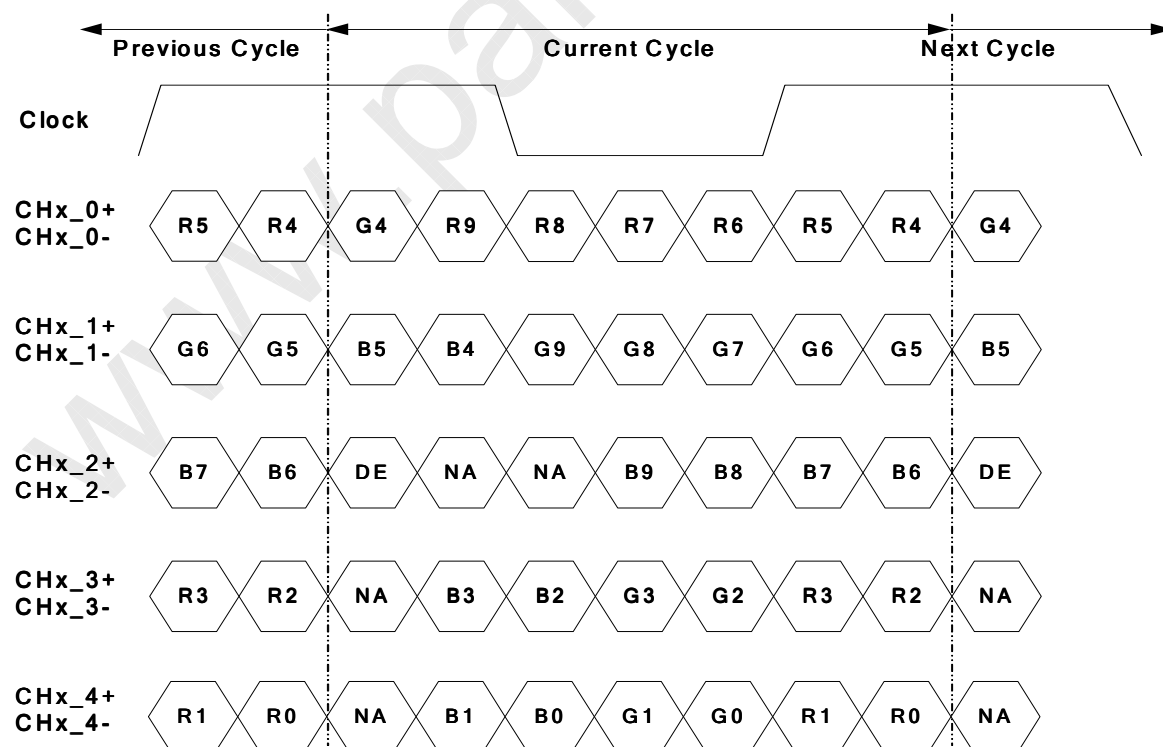
Note 1: All GND (ground) pins should be connected together and should also be connected to the LCD's metal frame.

Note 2: All V_{DD} (power input) pins should be connected together.

Note 3: All Reserved pins should be open without voltage input.

LVDS Option = High/Open→NS


Note: x = 1, 2, 3, 4...

LVDS Option = Low→JEIDA


Note: x = 1, 2, 3, 4...

3.3 Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	1096	1130	1392	Th
	Active	Tdisp (v)	1080			Th
	Blanking	Tblk (v)	16	50	312	Th
Horizontal Section	Period	Th	540	570	580	Tclk
	Active	Tdisp (h)	480			Tclk
	Blanking	Tblk (h)	60	90	100	Tclk
Clock	Frequency	Fclk=1/Tclk	64.8	77.29	80.74	MHz
Vertical Frequency	Frequency	Fv	94	120	122	Hz
Horizontal Frequency	Frequency	Fh	120	135.6	139.2	KHz

Notes:

(1) Display position is specific by the rise of DE signal only.

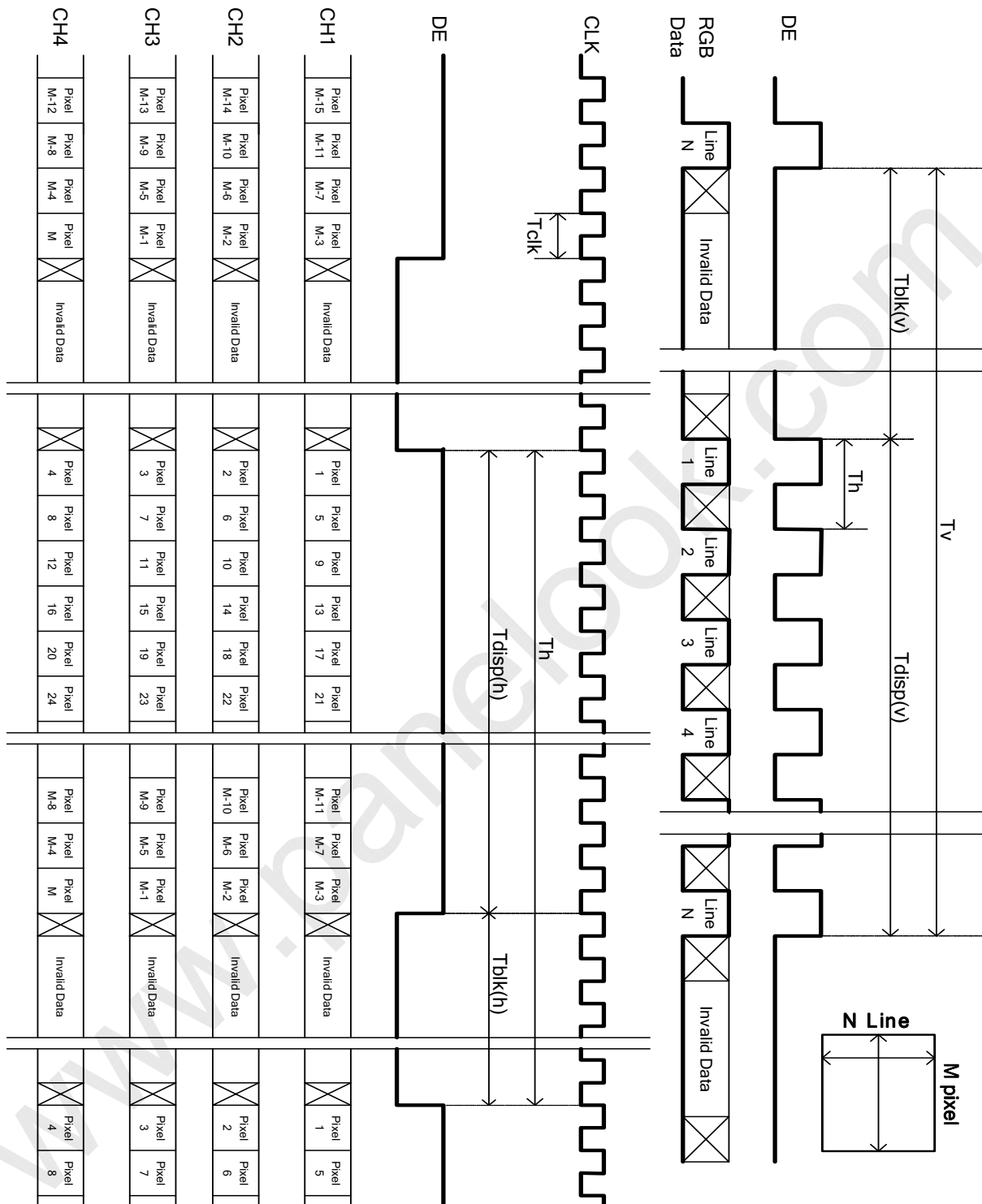
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2) Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3) If a period of DE “High” is less than 1920 DCLK or less than 1080 lines, the rest of the screen displays black.

(4) The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

3.4 Signal Timing Waveforms



3.5 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Color Data Reference

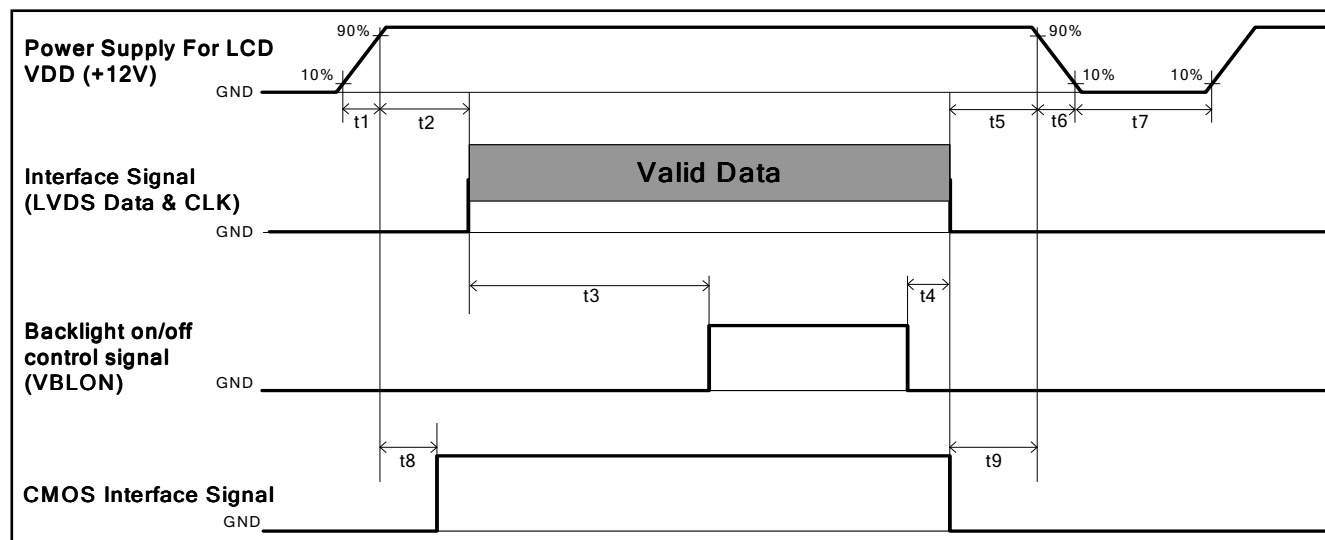
Color		Input Color Data																															
		RED										GREEN										BLUE											
		MSB					LSB					MSB					LSB					MSB						LSB					
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0		
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0		
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1		
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1		
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0		
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0		

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0		
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0		
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0		
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1		

3.6 Power Sequence for LCD (TBD)



Parameter	Values			Unit
	Min.	Type.	Max.	
t_1	0.4	---	30	ms
t_2	0.1	---	50	ms
t_3	450	---	---	ms
t_4	0 ^{*1}	---	---	ms
t_5	0	---	---	ms
t_6	---	---	--- ^{*2}	ms
t_7	500	---	---	ms
t_8	10 ^{*3}	---	50	ms
t_9	0	---	---	ms

Note:

- (1) $t_4=0$: concern for residual pattern before BLU turn off.
- (2) t_6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)
- (3) When CMOS Interface signal is N.C. (no connection), opened in Transmitted end, t_8 timing spec can be negligible.

3.8 Backlight Specification

The backlight unit contains 8pcs LED lightbar

3.8.1 Electrical specification

	Item	Symbol		Condition	Spec			Unit	Note
					Min	Typ	Max		
1	Input Voltage	VDDB		-	22.8	24	25.2	VDC	-
2	Input Current	I _{DDB}		VDDB=24V		8.73	9.58	ADC (rms)	1
3	Input Power	P _{DDB}		VDDB=24V		209.6	229.9	W	1
4	Inrush Current	I _{RUSH}		VDDB=24V			13	ADC (peak)	2
5	On/Off control voltage	V _{BLON}	ON	VDDB=24V	2	-	3.3	VDC	-
			OFF		0	-	0.8		3
6	On/Off control current	I _{BLON}		VDDB=24V	-	-	1.5	mA	-
7	External PWM Control Voltage	V _{EPWM}	MAX	VDDB=24V	2	-	3.3	VDC	-
			MIN	VDDB=24V	0	-	0.8		-
8	External PWM Control Current	I _{EPWM}		VDDB=24V	-	-	2	mADC	-
9	External PWM Duty ratio	D _{EPWM}		VDDB=24V	5	-	100	%	4,5
10	External PWM Frequency	F _{EPWM}		VDDB=24V	140	180	240	Hz	4,5
11	DET status signal	DET	HI	VDDB=24V	Open Collector			VDC	6
			Lo		0	-	0.8	VDC	6
12	Input Impedance	R _{in}		VDDB=24V	300			Kohm	

Note 1 : Dimming ratio= 100% (MAX) (Ta=25±5℃, Turn on for 45minutes)

Note 2: Measurement condition Rising time = 20ms (VDDB : 10%~90%);

Note 3: When BLU off (VDDB = 24V , VBLON = 0V) , IDDB (max) = 0.1A

Note 4: Less than 5% dimming control is functional well and no backlight shutdown happened

Note 5: D_EPWM and F_EPWM are available only at 2D mode

Note 6: Normal : 0~0.8V ; Abnormal : Open collector

3.8.2 Input Pin Assignment

14pin pin assignment

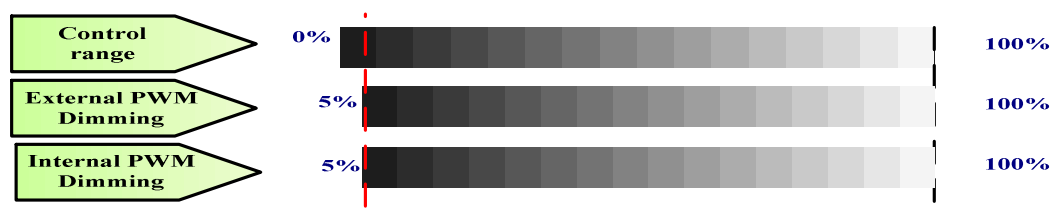
Connector: CI0114M1HR0-NH or equivalent

Pin NO.	Symbol	Pin Configuration (function)
1	VDDDB	Operating Voltage Supply, +24V DC regulated
2	VDDDB	Operating Voltage Supply, +24V DC regulated
3	VDDDB	Operating Voltage Supply, +24V DC regulated
4	VDDDB	Operating Voltage Supply, +24V DC regulated
5	VDDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	DET	BLU status detection: Normal : 0~0.8V ; Abnormal : Open collector (Recommend Pull high R > 10K, VDD = 3.3V)
12	VBLON	BL On-Off control High/Open (2.0V~3.3V) for BL On, Low (0~0.8V/GND) for off
13	NC	NC
14	External PWM (PDIM) (*)	External PWM (5%~100% Duty, open for 100%) < NC ; at Internal PWM mode>

12pin pin assignment

Connector: CI0112M1HR0-NH

Pin NO.	Symbol	Pin Configuration (function)
1	VDDDB	Operating Voltage Supply, +24V DC regulated
2	VDDDB	Operating Voltage Supply, +24V DC regulated
3	VDDDB	Operating Voltage Supply, +24V DC regulated
4	VDDDB	Operating Voltage Supply, +24V DC regulated
5	VDDDB	Operating Voltage Supply, +24V DC regulated
6	BLGND	Ground and Current Return
7	BLGND	Ground and Current Return
8	BLGND	Ground and Current Return
9	BLGND	Ground and Current Return
10	BLGND	Ground and Current Return
11	NC	NC
12	NC	NC

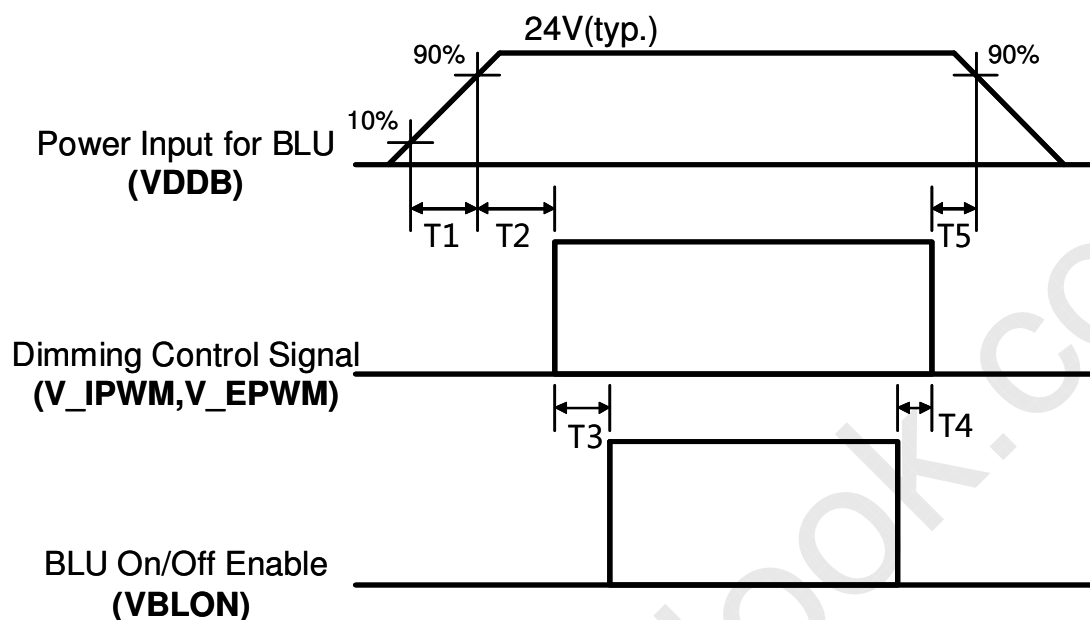


PWM Dimming : include Internal and External PWM Dimming

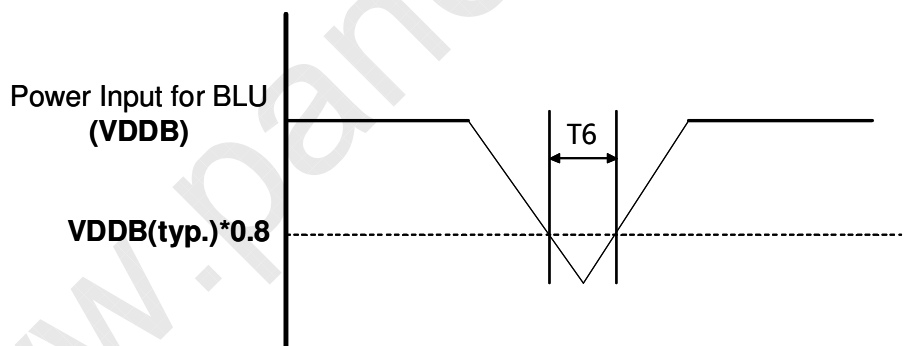
(Note*) IF External PWM function **less than 5%** dimming ratio. Judge condition as below:

- (1) Backlight module must be lighted ON normally.
- (2) All protection function must work normally.
- (3) Uniformity and flicker could NOT be guaranteed

3.8.3 Power Sequence for Backlight



Dip condition for LED Backlight

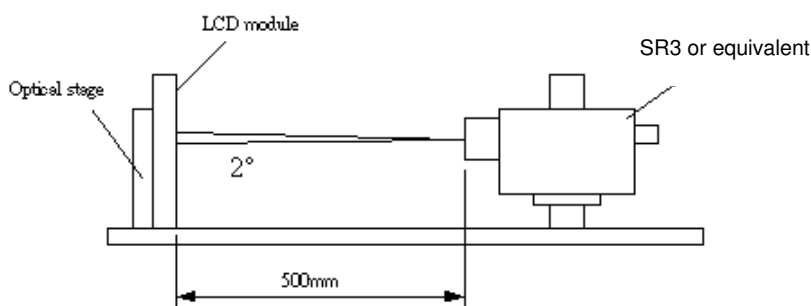


Parameter	Value			Units
	Min	Typ	Max	
T1	20	-	-	ms
T2	500	-	-	ms
T3	250	-	-	ms
T4	0	-	-	ms
T5	1	-	-	ms
T6	-	-	10	ms

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of ϕ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio(2D)		CR	3200	4000	--		1
Surface Luminance (White)		L _{WH}	280	360	--	cd/m ²	2
Luminance Variation		$\delta_{\text{WHITE}(9P)}$	--	--	1.33		3
Response Time (G to G)		T _γ	--	5.5	--	Ms	4
Color Gamut		NTSC		72		%	
Color Coordinates							
	Red	R _x	Typ.-0.03	0.640	Typ.+0.03		
		R _y		0.330			
	Green	G _x		0.310			
		G _y		0.620			
	Blue	B _x		0.150			
		B _y		0.050			
	White	W _x		0.280			
		W _y		0.290			
Viewing Angle							5
	x axis, right($\phi=0^\circ$)	θ_r	--	89	--	degree	
	x axis, left($\phi=180^\circ$)	θ_l	--	89	--	degree	
	y axis, up($\phi=90^\circ$)	θ_u	--	89	--	degree	
	y axis, down ($\phi=270^\circ$)	θ_d	--	89	--	degree	
	x axis, left + right	$\theta_l + \theta_r$			100	degree	6,7

Note:

1. Contrast Ratio (CR) is defined mathematically as:

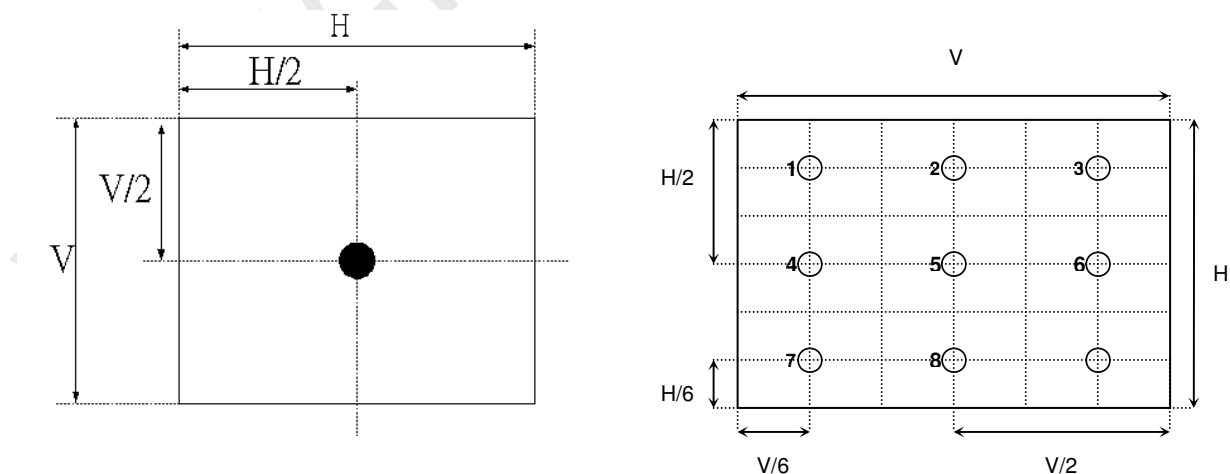
$$\text{Contrast Ratio} = \frac{\text{Surface Luminance of } L_{\text{on5}}}{\text{Surface Luminance of } L_{\text{off5}}}$$

- Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see FIG 2.
- The variation in surface luminance, δWHITE is defined (center of Screen) as:

$$\delta_{\text{WHITE(9P)}} = \text{Maximum}(L_{\text{on1}}, L_{\text{on2}}, \dots, L_{\text{on9}}) / \text{Minimum}(L_{\text{on1}}, L_{\text{on2}}, \dots, L_{\text{on9}})$$
- Response time T_{γ} is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on $F_v=60\text{Hz}$ to optimize. From more information see FIG 3.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

- Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG4.
- head in 0 degrees vertical angle from mid axis

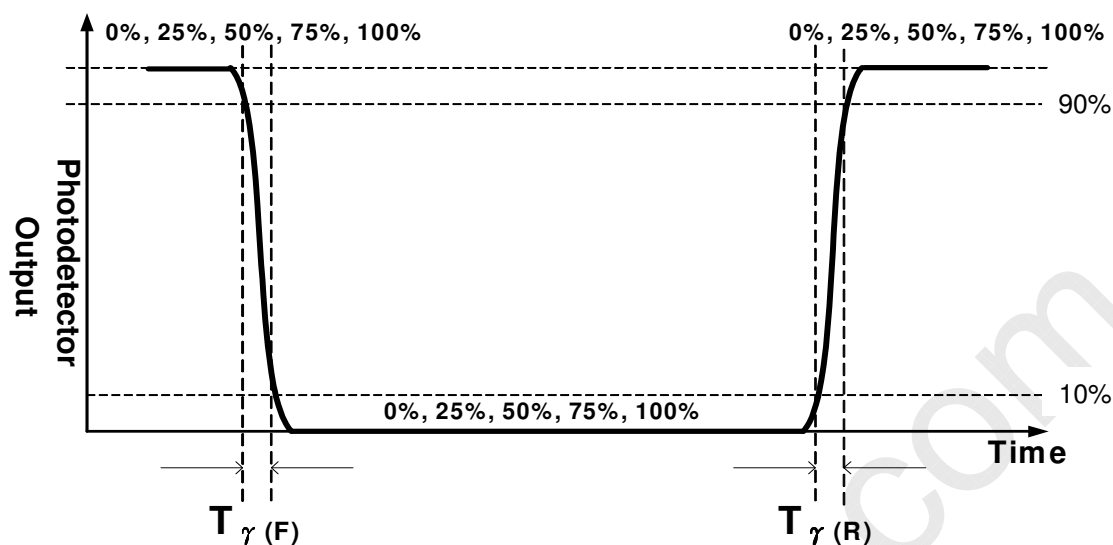
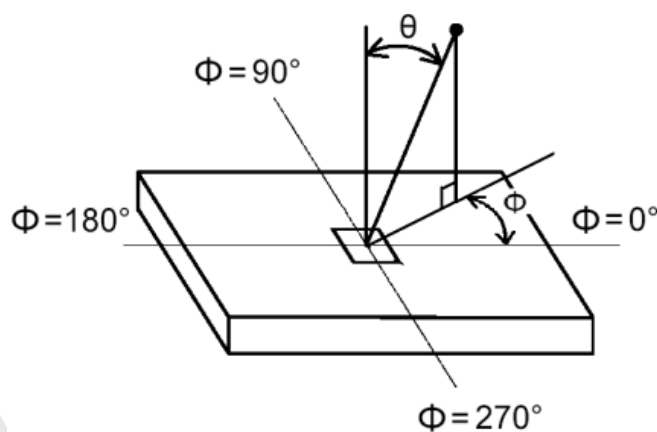
FIG. 2 Luminance

FIG.3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “any level of grey(bright) “ and “any level of gray(dark)”.

Any level of gray (Bright)

Any level of gray (Dark)

Any level of gray (Bright)

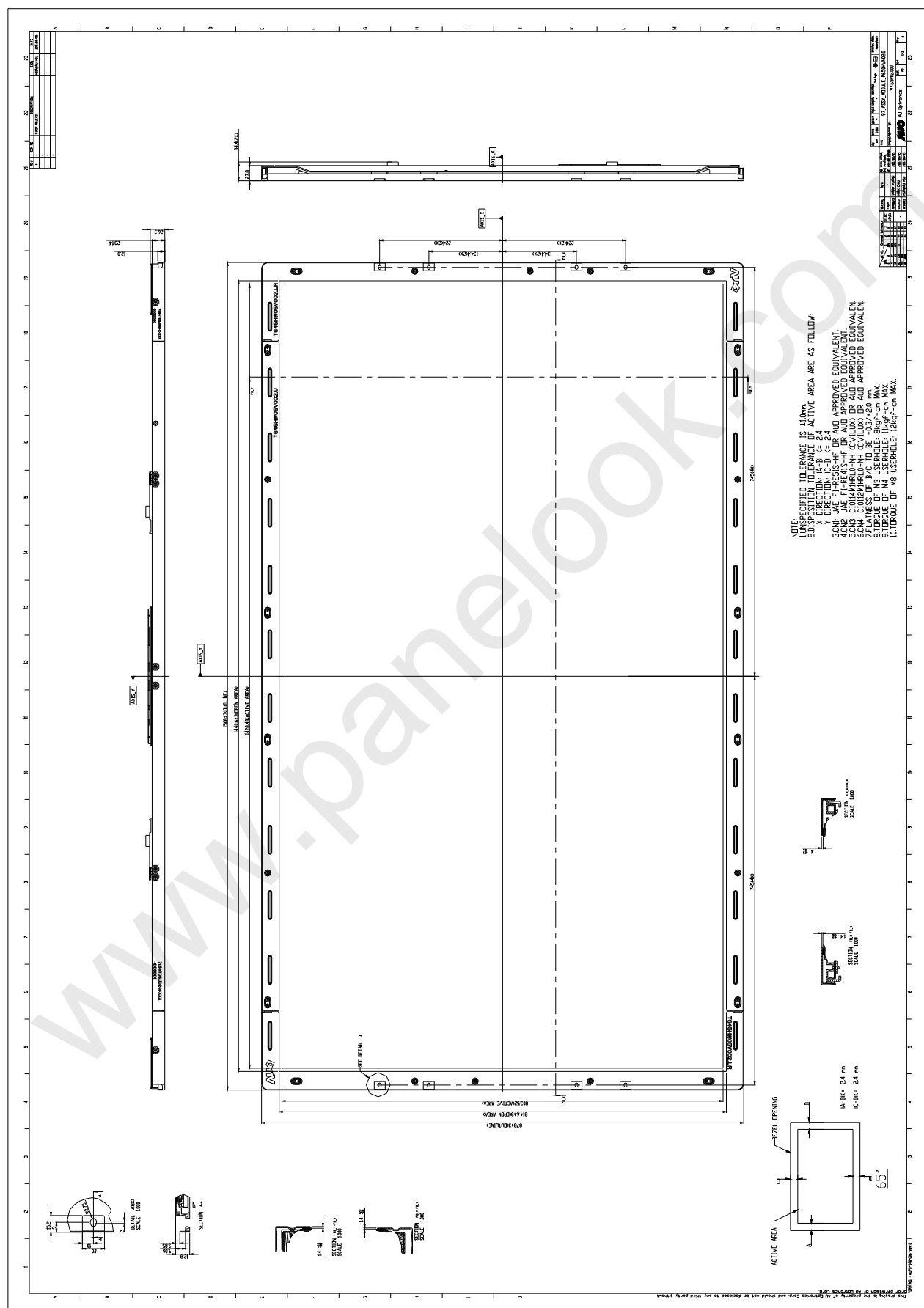
**FIG.4 Viewing Angle**

5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model P650HVN02.0. In addition the figures in the next page are detailed mechanical drawing of the LCD.

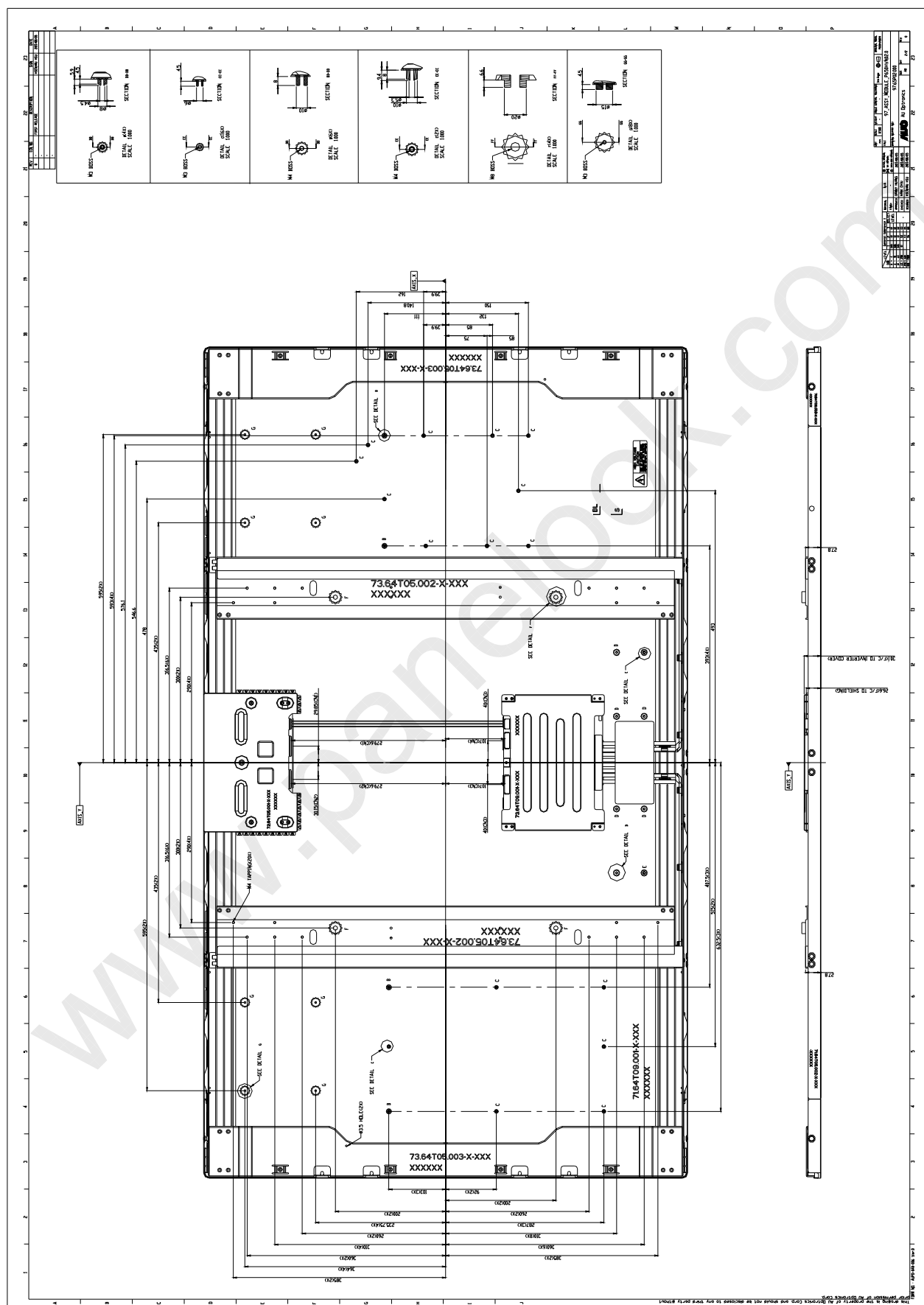
Outline Dimension	Horizontal	1508.0mm
	Vertical	878.0mm
	Depth	12.8mm (thinnest)
Bezel Opening	Horizontal	1440.6 mm
	Vertical	814.6 mm
Active Display Area	Horizontal	1428.48 mm
	Vertical	803.52 mm
Weight	33,000 g (Typ.)	
Surface Treatment	AG, 3H	

Front View





Back View



6. Reliability Test Items

	Test Item	Q'ty	Condition
1	High temperature storage test	3	60℃, 300hrs
2	Low temperature storage test	3	-20℃, 300hrs
3	High temperature operation test	3	50℃, 300hrs
4	Low temperature operation test	3	-5℃, 300hrs
7	Vibration test (With carton)	6	Random wave (1.05G RMS, 10-200Hz) 10mins/ Per each X,Y,Z axes
8	Drop test (With carton)	6	Height: 25.4 cm Direction: Only bottom flat (ASTMD4169-I)



7. International Standard

7.1 Safety

- (1) UL 60950-1, UL 60065; Standard for Safety of Information Technology Equipment Including electrical Business Equipment.
- (2) IEC 60950-1 : 2001, IEC 60065:2001 ; Standard for Safety of International Electrotechnical Commission
- (3) EN 60950 : 2001+A11, EN 60065:2002+A1:2006; European Committee for Electrotechnical Standardization (CENELEC), EUROPEAN STANDARD for Safety of Information Technology Equipment Including Electrical Business Equipment.

7.2 EMC

- (1) ANSI C63.4 "Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. "American National standards Institute(ANSI), 1992
- (2) C.I.S.P.R "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." International Special committee on Radio Interference.
- (3) EN 55022 "Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment." European Committee for Electrotechnical Standardization. (CENELEC), 1998

8. Packing

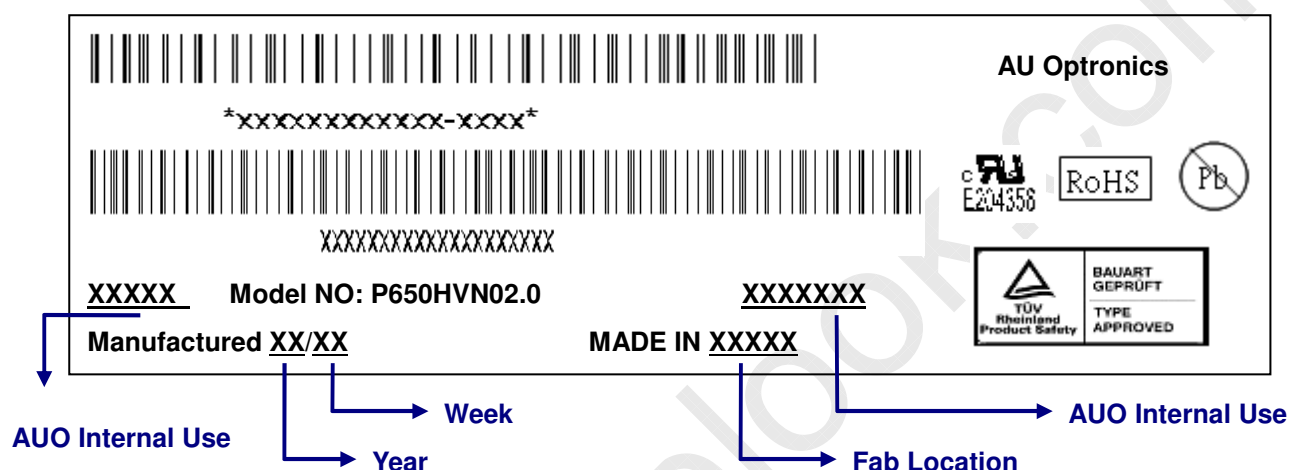
8-1 Definition of Label :

A. Panel Label:

XXXXXXXXXXXX-XXXX

Panel Unique ID

AUO Internal Use



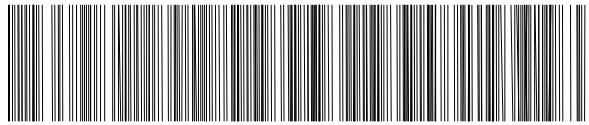
Green mark description

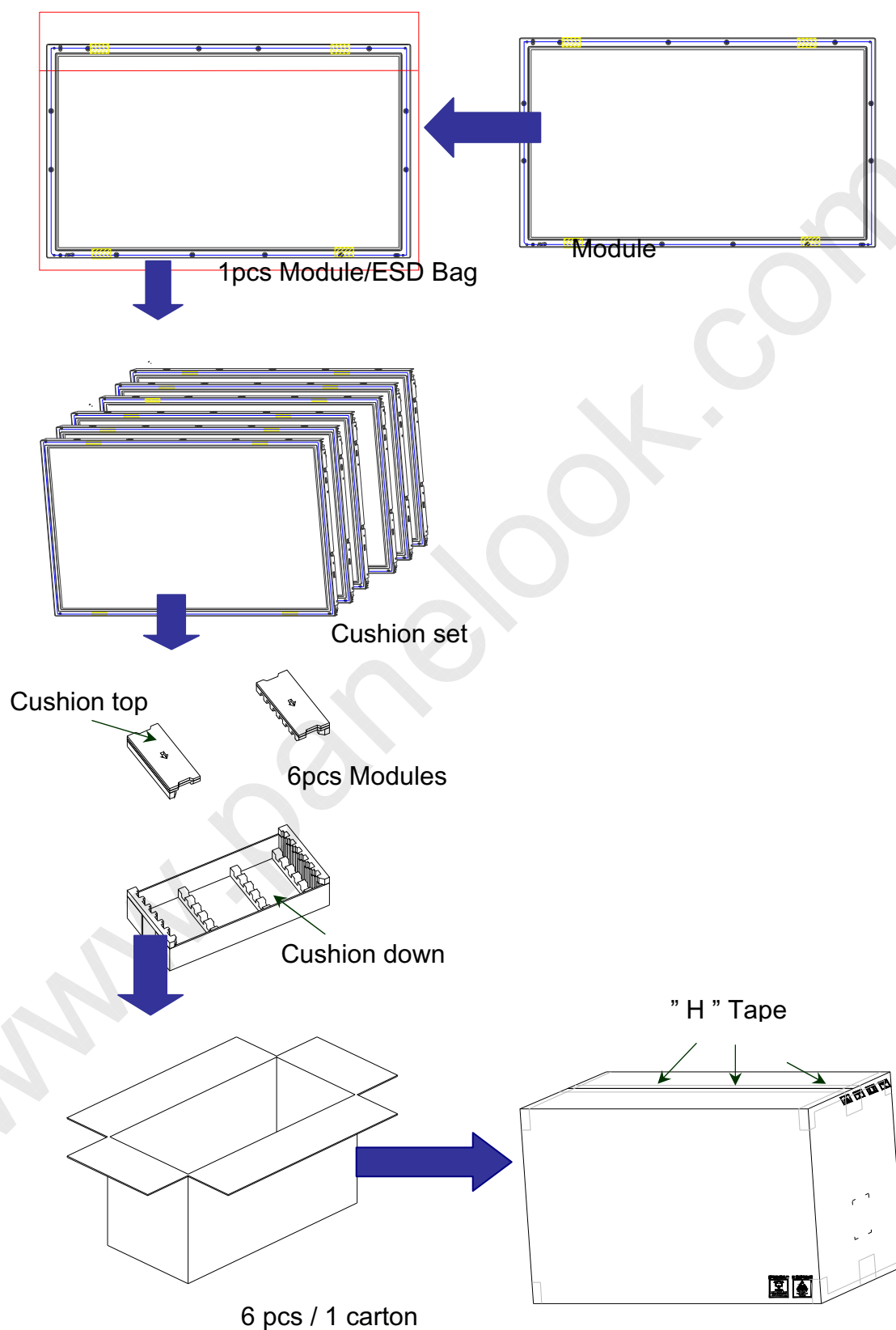
(1) For Pb Free Product, AUO will add  for identification.

(2) For RoHS compatible products, AUO will add  for identification.

Note: The green Mark will be present only when the green documents have been ready by AUO internal green team. (definition of green design follows the AUO green design checklist.)

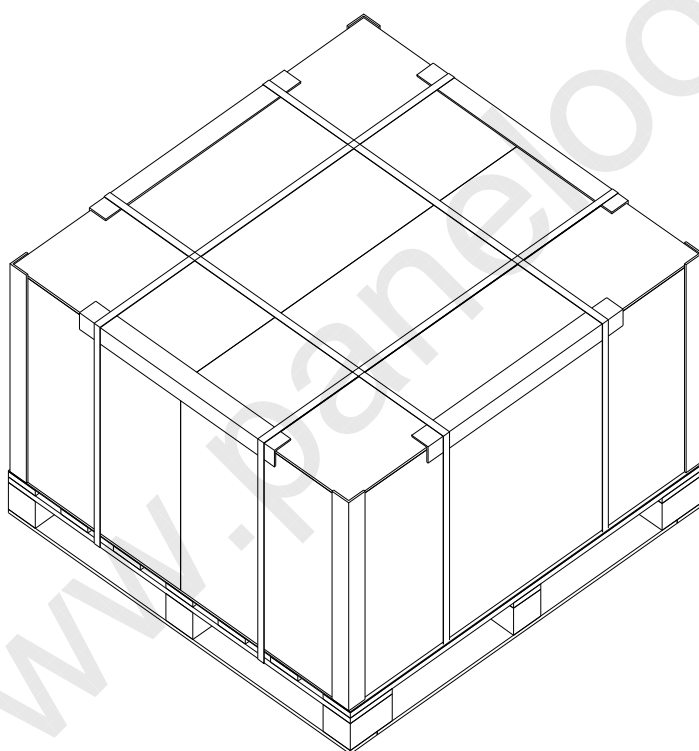
B. Carton Label:

AU Optonics	QTY :6		
MODEL NO: P650HVN02.0			
PART NO: 97.65P02.XXX			
CUSTOMER NO:			
CARTON NO:			
Made in XXXXXX	*XXXXX-XXXXXXXXXX*		

**8-2 Packing Methods:**

8-3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing Box	6pcs/box	1634(L)mm*555(W)mm*1035(H)mm	196	
2	Pallet	1	1660(L)mm*1150(W)mm*138(H)mm	20	
3	Boxes per Pallet	2 boxes/Pallet (By Air) ; 2 Boxes/Pallet (By Sea)			
4	Panels per Pallet	12 pcs/pallet(By Air) ; 12 pcs/Pallet (By Sea)			
5	Pallet after packing	12 (by Air)	1660(L)mm*1150(W)mm*1173(H)mm	412(by Air)	
		24 (by Sea)	1660(L)mm*1150(W)mm*2346(H)mm	824(by Sea)	40ft HQ



9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1 MOUNTING PRECAUTIONS

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.

9-2 OPERATING PRECAUTIONS

- (1) The device listed in the product specification sheets was designed and manufactured for TV application
- (2) The spike noise causes the mis-operation of circuits. It should be lower than following voltage:
 $V = \pm 200\text{mV}$ (Over and under shoot voltage)
- (3) Response time depends on the temperature. (In lower temperature, it becomes longer..)
- (4) Brightness of LED depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.
- (5) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (6) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (7) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall

be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.

9-3 ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

9-4 PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5 STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

9-6 HANDLING PRECAUTIONS FOR PROTECTION FILM

- (1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
- (3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.